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EXAMINER	
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ART UNIT	PAPER NUMBER
2614	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/738,719	GRABER ET AL.	
	Examiner	Art Unit	
	Michael R Shannon	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The "Related Patents/Applications" sections makes reference to "serial/patent number ******, entitled 'Multi-Mode Video Processor'", this should be corrected to contain the appropriate serial number, which is most likely 09738099.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 13, 17, 27, and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Dunn et al (US Pat. No. 6,154,772), cited by examiner.

With regards to claim 1, the claimed integrated video distribution system for distributing video signals from a plurality of sources is met as follows: The claimed control bus is met by the control channel, which is present on the communication channel 16, of figure 1 and by control lines 1011 of Figure 14. As described in column 19, lines 48-56 and column 20, lines 46-49, the control channel 1011 is used to control

system operation. The claimed video digitizer arrangement coupled to the control bus and having a plurality of analog video input ports and a plurality of digital video output ports, the digitizer arrangement configured and arranged to convert analog video signals to digital video data in YCrCb format at a first clock rate, each output port coupled to a respective first set of signal lines is met by MPEG-2 encoder 109, which converts received (input) analog broadcasts into (output) digitally compressed video signals. Column 7, lines 24-31 and lines 48-54 teach the use of the aforementioned MPEG-2 encoder(s). The claimed multiplexer arrangement having a plurality of output ports, each coupled to a respective second set of signal lines, the multiplexer configured and arranged to multiplex the digital video data at a second clock rate that is less than the first clock rate, wherein a number of signal lines in each first set is greater than a number of signal lines in each second set is met by the multiplexer 111 of Figure 4. As described in column 7, lines 48-54, the multiplexer serves to multiplex the now digitally encoded video onto the video control shelf. As can be seen in Figure 4, the multiplexer has multiple "M" inputs and it only has 1 output, therefore meeting the fact that the multiplexer has more input lines than output lines. The claimed digital video bus having a plurality of video channels coupled to respective output ports of the multiplexer, wherein each channel carries a stream of video data is met by the broadcast backplane 1200 (Figure 13). The multiplexer provides MPEG-2 digital video data in parallel format to the backplane. Column 19, lines 4-23 describe the broadcast backplane and its function as a digital video bus. The claimed plurality of terminal controllers responsive to an input signal coupled to the video bus and to the control bus, each terminal

controller having a data input port and a video output port and configured and arranged to select a subset of the streams of video data for output are met by the UAA modules 1000. The UAA modules function as access adapters for users to receive digital video content from the backplane and deliver the video programming to the customer as requested. Column 18, line 54 – column 19, line 23 describe, in detail, the ability for the UAA modules, acting as terminal controllers, to take input from the user and output the appropriate video content from the broadcast backplane to the user.

With regards to claim 2, Dunn teaches all of that which is discussed above with regards to claim 1. Dunn further teaches the claimed control signals being received at the UAA modules (terminal controllers) via input ports. According to column 19, lines 48-56, the UAA modules allow for user input via a control channel received at the UAA module.

With regards to claim 3, Dunn teaches all of that which is discussed above with regards to claim 1. The claimed backplane arrangement including the video bus and the control bus and having a plurality of expansion slots for connecting to the terminal controllers, each slot having pins coupled to the video bus and to the control bus is met by column 18, lines 4-49, wherein Dunn discloses a system which has a broadcast backplane 1200, including a digital video bus and control signals. He also discloses UAA module expandability, which can provide services to new customers and can be added (inserted into expansion slots) to the broadcast backplane.

With regards to claim 13, Dunn teaches all of that which is discussed above with regards to claim 1. The claimed digitizer arrangement comprising the following is met

as follows: The claimed plurality of digitizers coupled to the analog video input ports are met by MPEG-2 encoder(s) 109, which, as described in column 7, lines 24-54, serve to digitally encode the received analog video input. The claimed plurality of digital video receivers having input ports arranged to receive input digital video signals is met by the direct reception of the digital signals by the control shelf via connection 118, as described in column 7, lines 31-34. The claimed video bus controller arrangement having data input ports coupled to the digitizers and to the video receivers, the video bus controller configured and arranged to multiplex the video signals over the video channels of the video bus is met by the control shelf 200, which has multiple module pairs 300, used to process and arrange the video content received at the control shelf onto the digital video bus. Column 8, line 23 – column 9, line 15 serves as a description of the functionality of the control shelf 200.

With regards to claim 17, Dunn teaches all of that which is discussed above with regards to claim 1. The claimed plurality of display terminals coupled to the terminal controllers are met by the customer premises' for viewing video content, which are coupled to the UAA modules (terminal controllers). Figure 16 and column 21, line 66 – column 22, line 51 describe the customer premises' and its functions in detail. The claimed plurality of input devices coupled to the terminal controllers, the input devices arranged for input of control signals to the terminal controllers to select certain ones of the video signals for display at the display terminals is met by the IR remote control interface 1358, which serves to allow control communication to the UAA and is used for the purpose of selecting videos to be displayed at customer premises'.

With regards to claim 27, the claimed method for distributing video signals from a plurality of sources is met as follows: The claimed step of inputting a plurality of analog video signals is met by column 7, lines 24-54, wherein Dunn discloses the reception of multiple analog video signals. The claimed step of digitizing the plurality of analog video signals to respective streams of digital video data in YCrCb format at a first clock rate and outputting the digital video data on a first plurality of sets of signal lines is met by MPEG-2 encoder 109, which converts received (input) analog broadcasts into (output) digitally compressed video signals. Column 7, lines 24-31 and lines 48-54 teach the use of the aforementioned MPEG-2 encoder(s) to digitize the plurality of input analog signals. The claimed step of multiplexing the digital video data at a second clock rate and outputting the digital video data on a second plurality of sets of signal lines, wherein the second clock rate is less than the first clock rate and a number of signal lines in each set of the first plurality is greater than a number of signals in each set of the second plurality is met by the multiplexer 111 of Figure 4. As described in column 7, lines 48-54, the multiplexer serves to multiplex the now digitally encoded video onto the video control shelf. As can be seen in Figure 4, the multiplexer has multiple "M" inputs and it only has 1 output, therefore meeting the fact that the multiplexer has more input lines than output lines. The claimed step of selecting one or more of the streams of video data for output responsive to an input control signal and converting the selected streams of video data to analog video signals is met by column 18, line 66 – column 19, line 15, wherein Dunn teaches a system that responds to user input on a control channel by sending selected video content to the subscriber premises. The subscriber

premises then use a MPEG-2 chipset 1356 to decode and display the received digital video content (column 23, lines 36-41).

With regards to claim 31, the claimed distribution arrangement for distributing video signals from a plurality of sources is met as follows: The claimed means for inputting a plurality of analog video signals is met by column 7, lines 24-54, wherein Dunn discloses the reception of multiple analog video signals. The claimed means for digitizing the plurality of analog video signals to respective streams of digital video data in YCrCb format at a first clock rate and outputting the digital video data on a first plurality of sets of signal lines is met by MPEG-2 encoder 109, which converts received (input) analog broadcasts into (output) digitally compressed video signals. Column 7, lines 24-31 and lines 48-54 teach the use of the aforementioned MPEG-2 encoder(s) to digitize the plurality of input analog signals. The claimed means for multiplexing the digital video data at a second clock rate and outputting the digital video data on a second plurality of sets of signal lines, wherein the second clock rate is less than the first clock rate and a number of signal lines in each set of the first plurality is greater than a number of signals in each set of the second plurality is met by the multiplexer 111 of Figure 4. As described in column 7, lines 48-54, the multiplexer serves to multiplex the now digitally encoded video onto the video control shelf. As can be seen in Figure 4, the multiplexer has multiple "M" inputs and it only has 1 output, therefore meeting the fact that the multiplexer has more input lines than output lines. The claimed means for selecting one or more of the streams of video data for output responsive to an input control signal and converting the selected streams of video data to analog

video signals is met by column 18, line 66 – column 19, line 15, wherein Dunn teaches a system that responds to user input on a control channel by sending selected video content to the subscriber premises. The subscriber premises then use a MPEG-2 chipset 1356 to decode and display the received digital video content (column 23, lines 36-41).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 6, 9-12, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunn et al (US Pat. No. 6,154,772), cited by examiner, in view of Chang et al (US Pat. No. 6,791,601), cited by examiner.

With regards to claim 4, Dunn teaches all of that which is discussed above with regards to claim 1. Dunn does not expressly disclose a fail-safe video subsystem having a plurality of video signal input ports and a plurality of output ports, wherein selected ones of the input ports are coupled to output ports of the terminal controllers, and others of the input ports are arranged to be coupled to alternative video sources, wherein the fail-safe video subsystem is configured and arranged to provide on the output ports video signals from the alternative video sources in absence of power to the fail-safe video subsystem. Chang discloses an endoscopic camera system that utilizes

a fail-safe mechanism 51. As described in column 6, lines 10-60, and Figure 5, the fail-safe mechanism is used to route video input past the CPU in case of a power failure. During normal operation, the Video In signal is routed through the CPU, but upon power loss at the CPU, the fail-safe switch is actuated to route the Video In signal past the CPU and instead, directly to output. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the fail-safe mechanism, as taught by Chang, into the system taught by Dunn, in order to ensure that there is no appreciable interruption in the display of the video on the external monitor and that there is a constant feed of live video to the subscriber/user location in case of an otherwise disabling power failure.

With regards to claim 6, Dunn and Chang teach all of that which is discussed above with regards to claim 4. Dunn further teaches all of that which is discussed in claim 6. The claimed digitizer arrangement comprising the following is met as follows: The claimed plurality of digitizers coupled to the analog video input ports are met by MPEG-2 encoder(s) 109, which, as described in column 7, lines 24-54, serve to digitally encode the received analog video input. The claimed plurality of digital video receivers having input ports arranged to receive input digital video signals is met by the direct reception of the digital signals by the control shelf via connection 118, as described in column 7, lines 31-34. The claimed video bus controller arrangement having data input ports coupled to the digitizers and to the video receivers, the video bus controller configured and arranged to multiplex the video signals over the video channels of the video bus is met by the control shelf 200, which has multiple module pairs 300, used to

process and arrange the video content received at the control shelf onto the digital video bus. Column 8, line 23 – column 9, line 15 serves as a description of the functionality of the control shelf 200.

With regards to claim 9, Dunn and Chang teach all of that which is discussed above with regards to claim 6. Dunn further teaches a system that can multiplex and combine programming so as to increase and fully utilize available bandwidth in the network (column 9, lines 5-15). The claimed video channels being comprised of a first and a second set of video channels, each channel of the first set having a number of signals sufficient for parallel transmission of multiple streams of monochrome video data is met by the transmission of multiple program groups (as discussed in column 9, lines 5-15), which can be monochrome vs. color, or any other form of grouping that is preferred for transmission. The claimed second set having a number of signal lines sufficient for transmission of a single stream of color video data is met by the same connection with the same program groups, which get multiplexed on the transmission line.

With regards to claim 10, Dunn and Chang teach all of that which is discussed above with regards to claim 4. Dunn further teaches all of that which is discussed in claim 10. The claimed plurality of display terminals coupled to the terminal controllers are met by the customer premises' for viewing video content, which are coupled to the UAA modules (terminal controllers). Figure 16 and column 21, line 66 – column 22, line 51 describe the customer premises' and its functions in detail. The claimed plurality of input devices coupled to the terminal controllers, the input devices arranged for input of

control signals to the terminal controllers to select certain ones of the video signals for display at the display terminals is met by the IR remote control interface 1358, which serves to allow control communication to the UAA and is used for the purpose of selecting videos to be displayed at customer premises'.

With regards to claim 11, Dunn and Change teach all of that which is discussed above with regards to claim 10. Dunn does not expressly disclose an input device being a point-and-click device, however, he does suggest user input at the subscriber premises. Chang specifically points out the use of a pointing device for user input in Figure 4. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the point-and-click device of Chang into the system of Dunn, in order to use a standard user input device, which users area familiar with and can be easily implemented in any system.

With regards to claim 12, Dunn and Change teach all of that which is discussed above with regards to claim 10. Dunn does not expressly disclose an input device being a touchscreen, however, he does suggest user input at the subscriber premises. Chang specifically points out the use of a touchscreen for user input in Figure 4. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the touchscreen of Chang into the system of Dunn, in order to use a standard user input device, which users area familiar with and can be easily implemented in any system.

With regards to claim 18, Dunn teaches all of that which is discussed above with regards to claim 17. Dunn does not expressly disclose an input device being a point-

and-click device, however, he does suggest user input at the subscriber premises. Chang specifically points out the use of a pointing device for user input in Figure 4. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the point-and-click device of Chang into the system of Dunn, in order to use a standard user input device, which users area familiar with and can be easily implemented in any system.

With regards to claim 19, Dunn and Change teach all of that which is discussed above with regards to claim 18. Dunn does not expressly disclose an input device being a touchscreen, however, he does suggest user input at the subscriber premises. Chang specifically points out the use of a touchscreen for user input in Figure 4. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the touchscreen of Chang into the system of Dunn, in order to use a standard user input device, which users area familiar with and can be easily implemented in any system.

5. Claims 7, 8, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunn et al (US Pat. No. 6,154,772), cited by examiner, and Chang et al (US Pat. No. 6,791,601), cited by examiner.

With regards to claim 7, Dunn and Chang teach all of that which is discussed above with regards to claim 6. The claimed video bus controller arrangement having data input ports coupled to the digitizers and to the video receivers, the video bus controller configured and arranged to multiplex the video signals over the video

channels of the video bus is met by the control shelf 200, which has multiple module pairs 300, used to process and arrange the video content received at the control shelf onto the digital video bus. Column 8, line 23 – column 9, line 15 serves as a description of the functionality of the control shelf 200. The supervisory module 252, shell processor module 300, and video control module 250 are all implemented as separate entities within the system and all utilize some form of processor to accomplish their tasks. The reference, however, is silent as to the nature of the actual elements and processors used to fulfill the processes. The examiner gives Official Notice that it is notoriously well known in the art to use Field Programmable Gate Arrays (FPGAs) as typical logic chips for specialized applications, such as those mentioned above. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement Dunn and Chang utilizing FPGAs to accomplish these specialized tasks, in order to allow for flexibility, adaptability, and the ability to reprogram and upgrade (all of the benefits to such a system that FPGAs afford).

With regards to claim 8, Dunn and Chang teach all of that which is discussed above with regards to claim 7. Dunn discloses a system for coupling input analog signals (which have been digitized via the MPEG-2 encoder) to the video bus. He also discloses a system that coupled input digital signals directly to the video bus. Column 7, lines 24-34 provide a brief explanation of this teaching. Dunn is silent as to the coupling involved. He does disclose that certain parts are present (such as the video control shelf and connections 118), however, he does not expressly disclose how these couplings and connections are made. The examiner gives Official Notice that it is

notoriously well known in the art to use Field Programmable Gate Arrays (FPGAs) as typical logic chips for specialized applications, such as those mentioned above. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement Dunn and Chang utilizing FPGAs to accomplish these specialized tasks, in order to allow for flexibility, adaptability, and the ability to reprogram and upgrade (all of the benefits to such a system that FPGAs afford).

With regards to claim 14, Dunn teaches all of that which is discussed above with regards to claim 13. The claimed video bus controller arrangement having data input ports coupled to the digitizers and to the video receivers, the video bus controller configured and arranged to multiplex the video signals over the video channels of the video bus is met by the control shelf 200, which has multiple module pairs 300, used to process and arrange the video content received at the control shelf onto the digital video bus. Column 8, line 23 – column 9, line 15 serves as a description of the functionality of the control shelf 200. The supervisory module 252, shell processor module 300, and video control module 250 are all implemented as separate entities within the system and all utilize some form of processor to accomplish their tasks. The reference, however, is silent as to the nature of the actual elements and processors used to fulfill the processes. The examiner gives Official Notice that it is notoriously well known in the art to use Field Programmable Gate Arrays (FPGAs) as typical logic chips for specialized applications, such as those mentioned above. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement Dunn utilizing FPGAs to accomplish these specialized tasks, in order to allow for flexibility,

adaptability, and the ability to reprogram and upgrade (all of the benefits to such a system that FPGAs afford).

With regards to claim 15, Dunn teaches all of that which is discussed above with regards to claim 14. Dunn further discloses a system for coupling input analog signals (which have been digitized via the MPEG-2 encoder) to the video bus. He also discloses a system that couples input digital signals directly to the video bus. Column 7, lines 24-34 provide a brief explanation of this teaching. Dunn is silent as to the exact means of coupling involved. He does disclose that certain parts are present (such as the video control shelf and connections 118), however, he does not expressly disclose how these couplings and connections are made. The examiner gives Official Notice that it is notoriously well known in the art to use Field Programmable Gate Arrays (FPGAs) as typical logic chips for specialized applications, such as those mentioned above. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement Dunn utilizing FPGAs to accomplish these specialized tasks, in order to allow for flexibility, adaptability, and the ability to reprogram and upgrade (all of the benefits to such a system that FPGAs afford).

With regards to claim 16, Dunn and Chang teach all of that which is discussed above with regards to claim 14. Dunn further teaches a system that can multiplex and combine programming so as to increase and fully utilize available bandwidth in the network (column 9, lines 5-15). The claimed video channels being comprised of a first and a second set of video channels, each channel of the first set having a number of signals sufficient for parallel transmission of multiple streams of monochrome video data

is met by the transmission of multiple program groups (as discussed in column 9, lines 5-15), which can be monochrome vs. color, or any other form of grouping that is preferred for transmission. The claimed second set having a number of signal lines sufficient for transmission of a single stream of color video data is met by the same connection with the same program groups, which get multiplexed on the transmission line.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dunn et al (US Pat. No. 6,154,772), cited by examiner, in view of Chang et al (US Pat. No. 6,791,601), cited by examiner, in further view of Oftedahl et al (US Pat No. 6,449,768), cited by examiner. Dunn and Chang disclose all of that which is discussed above with regards to claim 4, however, the specifics of the fail-safe subsystem as claimed, are left out of both disclosures. The fail-safe video subsystem is met by Oftedahl as follows: The claimed first relay having a first and second output terminals and an input terminal arranged to be coupled to an associated one of the alternative video sources, wherein the first relay connects the input terminal to the first output terminal when in an energized state and connects the input terminal to the second output terminal when in a non-energized state is met by switch relay 44 (Figure 1). When switch relay 44 is in the energized state, it is in position A and routes the normal video to the combiner 38. When switch relay 44 is in the non-energized state, it is in position B and routes the backup video to the combiner 38. The claimed multiplexer having an output port, a first input port coupled to an associated one of the terminal controllers, and a second input

port coupled to the first output terminal of the first relay is met by Combiner 38, which serves to combine the output from switch relay 44 and switch relay 36. The first input is coupled to the backup through switch relay 44 and the second input port is coupled to the primary path (which also goes to switch relay 44) through switch relay 36. The claimed second relay having a first input terminal coupled to the output port of the multiplexer, a second input terminal coupled to the second output terminal of the first relay, and an output terminal coupled to an output port of the fail-safe video subsystem, wherein the second relay connects the first input terminal to the output terminal when in an energized state and connects the second input terminal to the output terminal when in a non-energized state is met by switch relay 36 (Figure 1). When switch relay 36 is in the energized state, it is in position A and routes the normal video to the combiner 38. When switch relay 36 is in the non-energized state, it is in position B and routes the backup video to the combiner 38.

7. Claims 20-26, and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dunn et al (US Pat. No. 6,154,772), cited by examiner, in view of Wicker et al (US Pat. No. 6,441,857), cited by examiner.

With regards to claim 20, Dunn teaches all of that which is discussed above with regards to claim 1. Dunn does not disclose any of the clock rate teachings, as discussed in claim 20. The claimed second clock rate being about half of that first clock rate is met by Wicker, wherein he teaches an encoder (digitizer) clock rate being commonly set at 13.5 MHz (column 12, lines 49-51) and a multiplexer with a clock rate

of 27 MHz (Figures 12 and 13). As can be seen, 13.5 MHz is exactly half that of the 27 MHz. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the clock ratios of Wicker into the system of Dunn, in order to allow for faster processing and for more throughput. Also, as is mentioned in the Wicker reference, the 13.5 MHz is in accordance with the NTSC standard.

With regards to claim 21, Dunn and Wicker teach all of that which is discussed above with regards to claim 20. Dunn does not disclose the a video data multiplexer arrangement generates data that defines a color pixel, each pixel defined by at least four words of data and a color video control code. This claim, however, is met by Wicker, wherein he teaches a 16-bit 4:2:2 YCrCb pixel data processing apparatus (column 10, lines 7-22). As can be seen, each pixel is defined by 4 4-byte words and a color video control code (see Figure 6). It would have been obvious to one or ordinary skill in the art at the time of the invention to implement to 16-bit 4:2:2 YCrCb pixel data processor into the multiplexer taught by Dunn, in order to allow for a standardized transmission scheme. YCrCb data is commonly known in the art and is a standard way of transmitting Luminance and Chrominance values, which define an image.

With regards to claim 22, Dunn and Wicker teach all of that which is discussed above with regards to claim 21. Dunn does not expressly disclose that the data words are transmitted on different clock edges. Wicker discloses a system that utilizes the rising and falling clock edges to send data words. Figure 6 shows how the data in the 16-bit YCrCb Mode is transmitted. The first and third data words (CrCb 0-7) are transmitted on the rising edge and the second and fourth data words (Y0-Y7) are

transmitted on the falling edge at a clock rate of 27 MHz. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the data transmission scheme of Wicker into the system of Dunn, in order to allow for faster transmission and, since 4:2:2 format takes two samples for luminance values and one sample for chrominance values, the whole process of utilizing the full clock pulse would provide a faster sampling process.

With regards to claim 23, Dunn and Wicker teach all of that which is discussed above with regards to claim 22. Dunn does not expressly disclose anything about the data words. Wicker discloses a system that uses the first and second words to define chroma red data, the third and fourth data words to define the chroma blue data, and all four data words to define the luma data. Column 10, lines 7-22 and Figure 6, show that the data is broken up into words and transmitted accordingly. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the Dunn system in order to transmit the chroma red, chroma blue, and luma data to define a pixel. This would have provided the benefit of a standard transmission scheme and the ability for the information to be easily transmitted without the need for a large amount of bandwidth.

With regards to claim 24, Dunn and Wicker teach all of that which is discussed above with regards to claim 23. Dunn does not disclose a specific frequency at which the data words are clocked at the multiplexer. Wicker, however, discloses a frequency of 27 MHz, which is double that utilized by the encoders. This meets the claimed data words being clocked at a frequency of 33 MHz, since 33 MHz and 27 MHz do not

provide a patentable distinction. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the specified frequency to clock data words into the multiplexer within the system as taught by Dunn in order to utilize a frequency that is double that of the encoder frequency and to allow the system to work at a higher clock rate.

With regards to claim 25, Dunn and Wicker teach all of that which is discussed above with regards to claim 20. Dunn does not disclose anything about the multiplexer arrangement generating data that defines monochrome pixels, each pixel being defined by a set of data words and a monochrome video control code. This claim, however, is met by Wicker, wherein he teaches a 16-bit 4:2:2 YCrCb pixel data processing apparatus (column 10, lines 7-22), which can also be used to process monochrome pixel data. As can be seen, each pixel is defined by 4, 4-byte words and a video control code (see Figure 6). It would have been obvious to one or ordinary skill in the art at the time of the invention to implement to 16-bit 4:2:2 YCrCb pixel data processor into the multiplexer taught by Dunn, in order to allow for a standardized transmission scheme. YCrCb data is commonly known in the art and is a standard way of transmitting Luminance and Chrominance values, which define an image.

With regards to claim 26, Dunn and Wicker teach all of that which is discussed above with regards to claim 25. Dunn does not expressly disclose the data words being transmitted on a rising clock edge and a falling clock edge. Wicker discloses a system that utilizes the rising and falling clock edges to send data words. Figure 6 shows how the data in the 16-bit YCrCb Mode is transmitted. The first data word (CrCb 0-7) is

transmitted on the rising edge and the second data word (Y0-Y7) is transmitted on the falling edge at a clock rate of 27 MHz. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the data transmission scheme of Wicker into the system of Dunn, in order to allow for faster transmission and, since 4:2:2 format takes two samples for luminance values and one sample for chrominance values, the whole process of utilizing the full clock pulse would provide a faster sampling process.

With regards to claim 28, teaches all of that which is discussed above with regards to claim 27. Dunn does not disclose the step of multiplexing the digital video data including generating data that defines a pixel with a set of data and a video control signal. This claim, however, is met by Wicker, wherein he teaches a 16-bit 4:2:2 YCrCb pixel data processing apparatus (column 10, lines 7-22). As can be seen, each pixel is defined by 4, 4-byte words and a color video control code (see Figure 6). It would have been obvious to one or ordinary skill in the art at the time of the invention to implement to 16-bit 4:2:2 YCrCb pixel data processor into the multiplexer taught by Dunn, in order to allow for a standardized multiplexing scheme. YCrCb data is commonly known in the art and is a standard way of transmitting Luminance and Chrominance values, which define an image.

With regards to claim 29, Dunn and Wicker teach all of that which is discussed above with regards to claim 28. Dunn does not expressly disclose that the data words are transmitted on different clock edges. Wicker discloses a system that utilizes the rising and falling clock edges to send data words. Figure 6 shows how the data in the

16-bit YCrCb Mode is transmitted. The first and third data words (CrCb 0-7) are transmitted on the rising edge and the second and fourth data words (Y0-Y7) are transmitted on the falling edge at a clock rate of 27 MHz. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the data transmission scheme of Wicker into the system of Dunn, in order to allow for faster transmission and, since 4:2:2 format takes two samples for luminance values and one sample for chrominance values, the whole process of utilizing the full clock pulse would provide a faster sampling process.

With regards to claim 30, Dunn and Wicker teach all of that which is discussed above with regards to claim 28. Dunn does not expressly disclose the data words being transmitted on a rising clock edge and a falling clock edge. Wicker discloses a system that utilizes the rising and falling clock edges to send data words. Figure 6 shows how the data in the 16-bit YCrCb Mode is transmitted. The first data word (CrCb 0-7) is transmitted on the rising edge and the second data word (Y0-Y7) is transmitted on the falling edge at a clock rate of 27 MHz. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the data transmission scheme of Wicker into the system of Dunn, in order to allow for faster transmission and, since 4:2:2 format takes two samples for luminance values and one sample for chrominance values, the whole process of utilizing the full clock pulse would provide a faster sampling process.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takamori (US Pat. No. 5,287, 186) discloses a switching apparatus for switching between two different sources of video information. His teachings can be implemented as a fail-safe system.

Sit et al (US Pat. No. 5,963,843) discloses another switching apparatus, which can read on a general fail-safe system.

Rodriguez (US Pat. No. 4,511,886) discloses a system for electronic video surveillance, with multiple cameras and one viewing location (though many could be added).

Oliver, Jr. (US Pat. No. 4,814,869) discloses a video surveillance system with a plurality of video camera outputs being multiplexed on a single path.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael R Shannon whose telephone number is 703-305-6955. The examiner can normally be reached on M-F 7:30-5:00, alternate Friday's off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on 703-305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Michael R Shannon
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September 30, 2004

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